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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,403	03/31/2004	Danny S. Barlow	M-15325 US	7974

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,403	BARLOW, DANNY S.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/31/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first feedback path determines the high voltage threshold, the Schmitt trigger further comprising a second feedback path that determines the low voltage threshold" (claim 7) and "the first feedback path comprises a first NMOS transistor having a terminal coupled to the at least one diode and wherein the second feedback path comprises a first PMOS transistor" (claim 8), "the at least one diode coupled between the drain terminal and a supply voltage terminal" (claim 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 11-13, 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Naura (U.S Patent No. 6,127,898).

Naura discloses in Figs. 2-5 a ring oscillator including:

Regarding claim 1:

a first feedback path (CP1, T5 feedback path) configured to determine one of the voltage thresholds; and

at least one diode (T11, Fig. 4) coupled to the first feedback path (CP1, T5 feedback path) such that an on-current through the first feedback path (CP1, T5 feedback path) is reduced as a supply voltage for the Schmitt trigger is reduced (because the claimed structure is fully met by Naura, this limitation will necessarily be inherent in Naura; as held by the court in In re Best, 195 USPQ 430)..

Regarding claim 2: the Schmitt trigger is a CMOS Schmitt trigger (see col. 1, lines 7-9).

Regarding claim 3: the first feedback path (CP1, T5 feedback path) is configured to determine the low voltage threshold, the Schmitt trigger further comprising: a second feedback path (CP2, T6 feedback path) configured to determine the high voltage threshold.

Regarding claim 4: the first feedback path (CP1, T5 feedback path) comprises a first PMOS transistor (T7) having a terminal coupled to the at least one diode (T11) and wherein the second feedback path (CP2, T6 feedback path) comprises a first NMOS transistor (T10).

Regarding claim 11: elements T1, T2 read on second and third PMOS transistors and elements T3, T4 read on second and third NMOS transistors all coupled in series between a supply voltage terminal (Vcc) and a ground terminal (Vss).

The method recited in claims 12-13 are inherent to the operation of the ring oscillator using CMOS technology of Naura.

Claims 15-16 are similarly rejected as above claims:

a first feedback path (CP1, T5 feedback path) configured to determine one of the voltage thresholds; and

means for reducing an on-current (Fig. 4) through the first feedback path (CP1, T5 feedback path) as a supply voltage for the Schmitt trigger is reduced (because the claimed structure is fully met by Naura, this limitation will necessarily be inherent in Naura; as held by the court in In re Best, 195 USPQ 430);

the first feedback path (CP1, T5 feedback path) comprises a first PMOS transistor (T7) and the means for reducing the on-current (Fig. 4) comprises at least one diode (T11).

Regarding claim 17: the at least one diode comprises a diode-connected PMOS transistor (T11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art depicted by the Applicant's Figs. 1 and 5 and further in view of Rodriguez et al (U.S Patent No. 6,703,882).

The prior art discloses in Fig. 1 a conventional Schmitt trigger including a first feedback path (feedback via transistor P3) as recited in claim 1.

What is not shown in the prior art, Figs. 1 and 5 is the limitation "at least one diode" recited in claim 1.

Rodriguez et al teach in Fig. 2 an improving CMOS inverter (220-230) having a diode-connected transistor (245) coupled between transistor 220 and ground for the purpose of reducing the turn off voltage.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to insert a diode between drain terminal of P3 and Ground

of the prior art as taught by Rodriguez's Fig. 2 for the purpose of reducing turn off voltage and limiting crossbar current duty cycle, thus increasing speed and reducing power consumption.

The prior art teaches the Schmitt trigger is a CMOS Schmitt trigger (100) as recited in claim 2.

Regarding claim 3: the first feedback path (feedback via P3) is configured to determine the low voltage threshold, the Schmitt trigger further comprising: a second feedback path (feedback via N3) configured to determine the high voltage threshold (see Fig. 2 of the prior art).

Regarding claim 4: the first feedback path comprises a first PMOS transistor (P3), the second feedback path comprises a first NMOS transistor (N3), same reasons applied to claim 1 is applied to claim 4 for "the at least one diode" limitation.

The same motivation applied to claim 1 is applied to claim 5 regarding the limitation "the at least one diode comprises a first diode and a second diode". It would have been obvious at the time the invention was made to a person having ordinary skill in the art to insert plurality of diode (first and second diodes) between the drain terminal of P3 and the ground of the prior art as taught by Rodriguez's Fig. 2 for the purpose of reducing more turn off voltage and limiting more crossbar current duty cycle, thus increasing speed and reducing power consumption.

Regarding claim 6: the terminal is a drain terminal (drain of P3), the at least one diode coupled between the drain terminal and a ground (same motivation applied to claim 1 is applied to this limitation).

Regarding the limitation recited in claims 7-10: the different recited in these claims are not a patentable one since it involves merely rearranging the chain of the circuit without any difference in operative result. Therefore, it would have been obvious at the time the invention was made for one skilled in the art to realize the circuit of the prior art, Fig. 1 using the particular connection recited in the claims 7-10 since these limitations drawn to a particular connection is seen as a design expedient that depends upon the desired output. Moreover, the same motivation applied to claim 1 is applied to the limitation "at least one diode" or "the at least one diode comprises a first diode and a second diode" recited in claims 8-10.

Regarding claim 11: elements P1, P2 read on a second and a third PMOS transistor and elements N2, N1 read on a second and a third NMOS transistor (the prior art, Fig. 1).

The method recited in claims 12-14 are similarly rejected as claims 1, 3, and 7.

Claim 15-16 are similarly rejected as claim 1:

a first feedback path (feedback via P3) (or feedback via P2 of Fig. 5), a first PMOS transistor (P3) (or P2, Fig. 5).

The prior art, Fig, 1 lacks "means for reducing an on-current" (claim 15), "the means for reducing the on current comprises at least one diode" (claim 16).

Rodriguez et al teach in Fig. 2 an improving CMOS inverter (220-230) having a diode-connected transistor (245) coupled between transistor 220 and ground for the purpose of reducing the turn off voltage.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to insert a diode between drain terminal of P3 and Ground of the prior art as taught by Rodriguez's Fig. 2 for the purpose of reducing turn off voltage and limiting crossbar current duty cycle, thus increasing speed and reducing power consumption.

Rodriguez et al show the at least diode comprises a diode-connected PMOS transistor (250) as recited in claim 17.

The same motivation applied to claims 15-16 is applied to claim 18.

Regarding claim 19: the prior art, Fig. 5 lacks "the diode-connected PMOS transistor couples between a supply voltage terminal and a source of the first PMOS transistor". The same motivation applied to above claims applied to this limitation.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to insert a diode between a supply voltage terminal (Vcc) and a source of the first PMOS transistor (P2) of the prior art, Fig. 5 as taught by Rodriguez's Fig. 2 of Rodriguez for the purpose of reducing turn off voltage and limiting crossbar current duty cycle, thus increasing speed and reducing power consumption.

Regarding claim 20:

the prior art, Fig. 5 shows a first inverter (P1, N1) to invert the input voltage (Vin) to provide an inverted output of an output terminal; and

a second inverter (INV) configured to invert the inverted output from the output terminal of the first inverter (P1, N1), wherein a drain of the first PMOS transistor (P2) couples to the output terminal of the first inverter (P1, N1)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

March 24, 2005